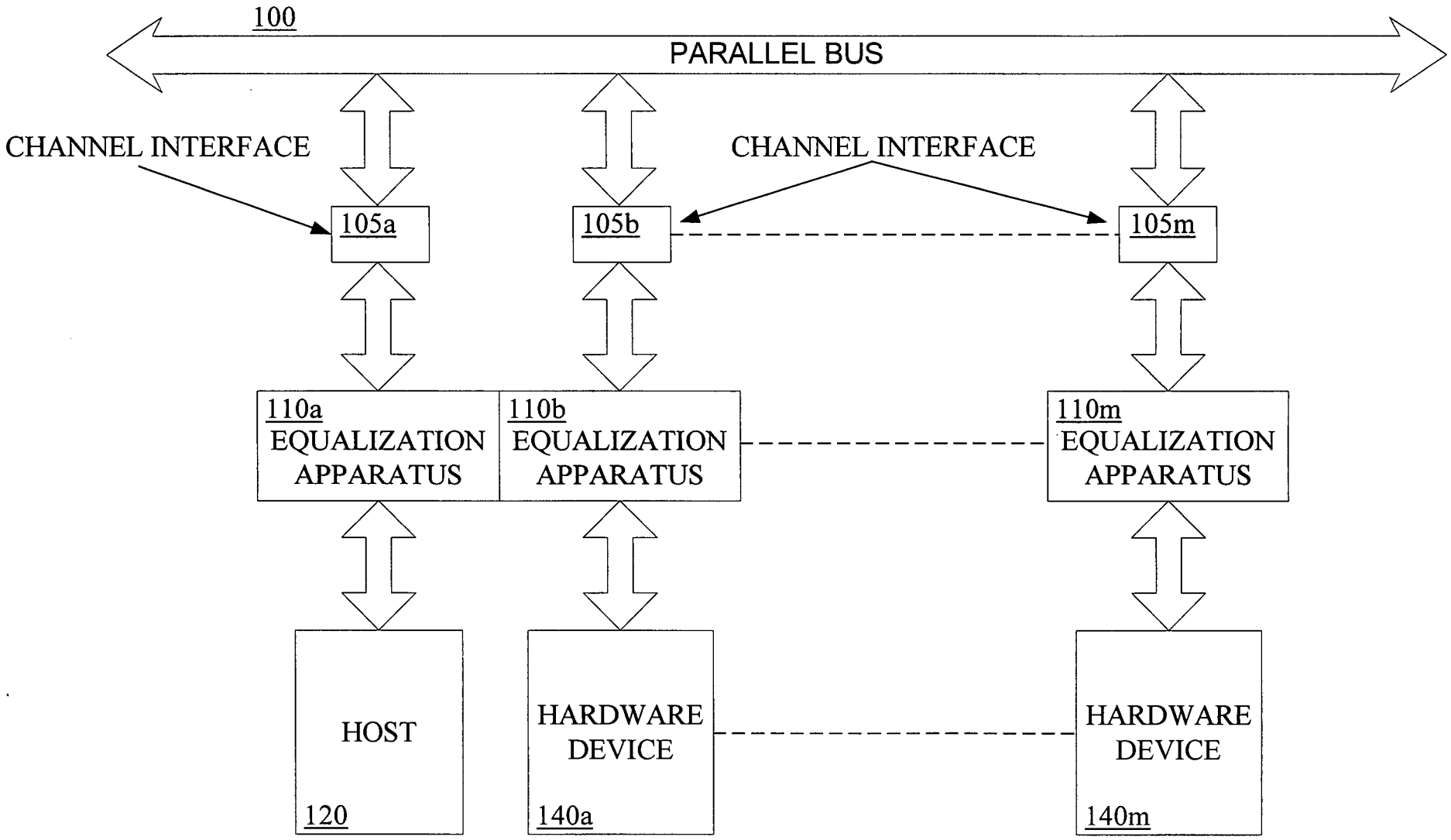

100
PARALLEL BUS
CHANNEL INTERFACE
CHANNEL INTERFACE
105a
105b
105m
110a
EQUALIZATION
APPARATUS
110b
EQUALIZATION
APPARATUS
110m
EQUALIZATION
APPARATUS
HOST
120
HARDWARE
DEVICE
140a
HARDWARE
DEVICE
140m

FIG. 1

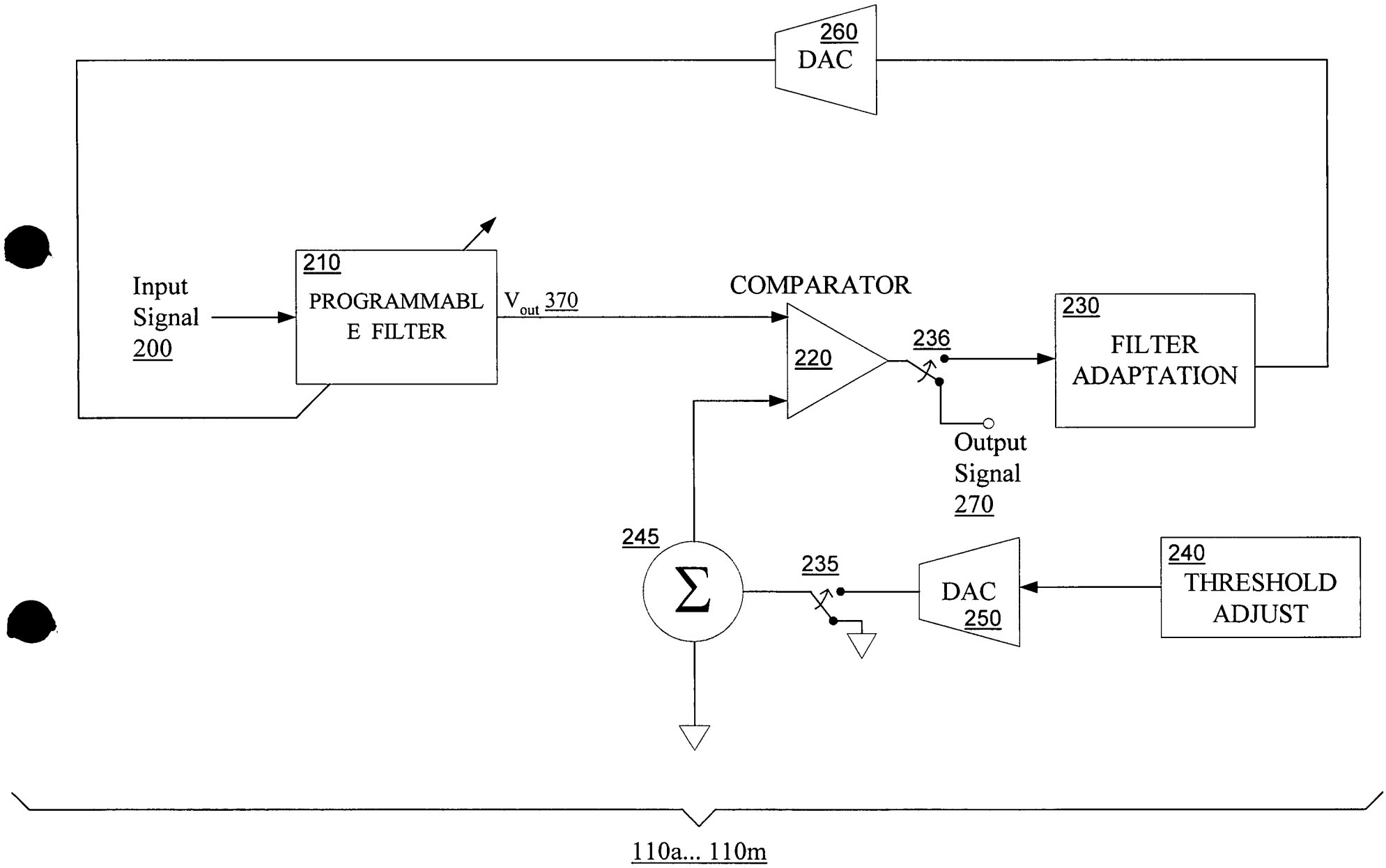
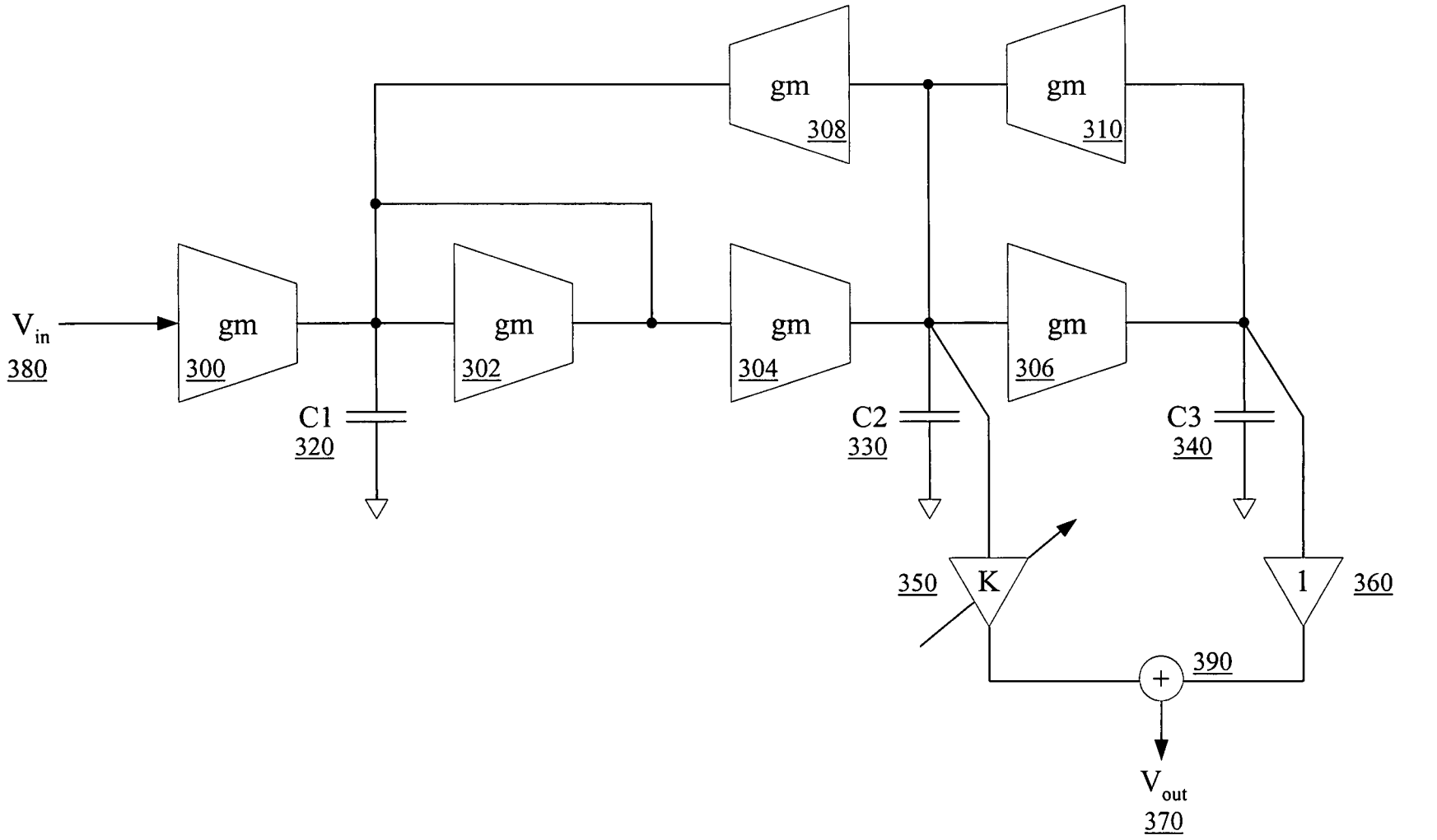

260
DAC
Input
Signal
200
210
PROGRAMMABL
E FILTER
V_{out} 370
COMPARATOR
220
236
230
FILTER
ADAPTATION
Output
Signal
270
245
Σ
235
DAC
250
240
THRESHOLD
ADJUST
110a... 110m

FIG. 2


gm
308
gm
310
V_{in}
380
gm
300
gm
302
gm
304
gm
306
C1
320
C2
330
C3
340
350
K
1
360
390
+
V_{out}
370

210

FIG. 3

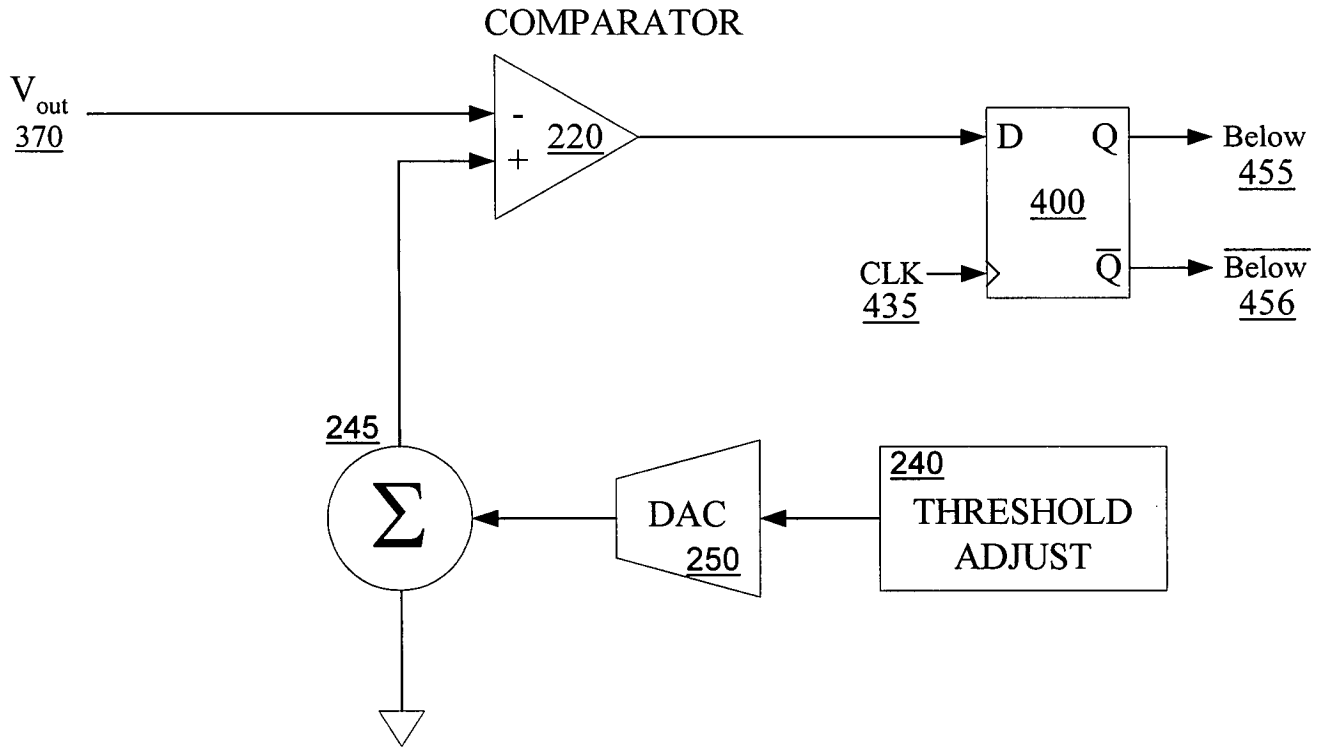
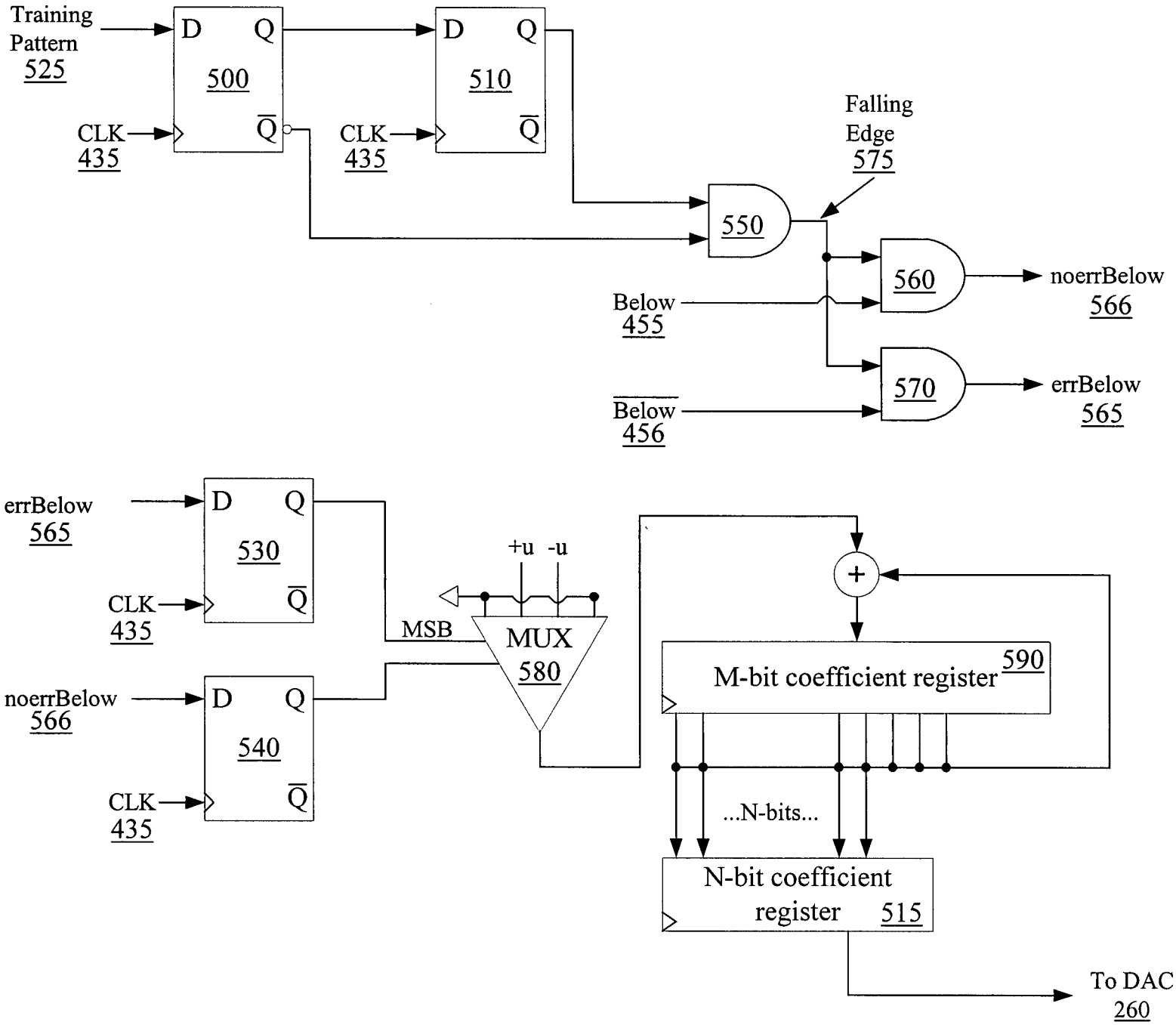


FIG. 4

D9650364 . 082503


Training Pattern 525
D
Q
500
CLK 435
510
Falling Edge 575
550
560
noerrBelow 566
Below 455
570
errBelow 565
Below 456
530
MSB
+u -u
MUX 580
M-bit coefficient register 590
noerrBelow 566
540
...N-bits...
N-bit coefficient register 515
To DAC 260

230 FIG. 5

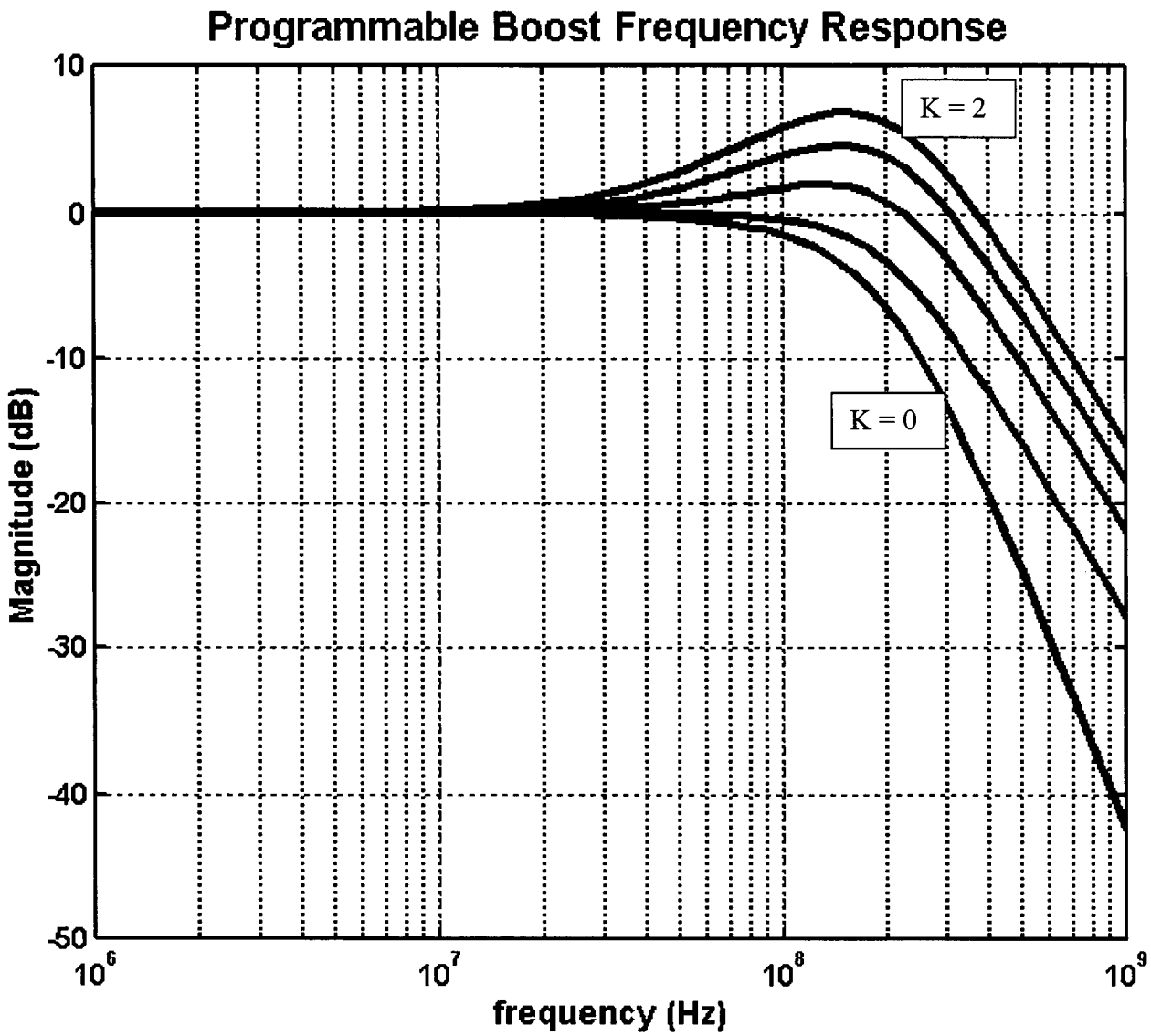


FIG. 6

05656964 . 062900

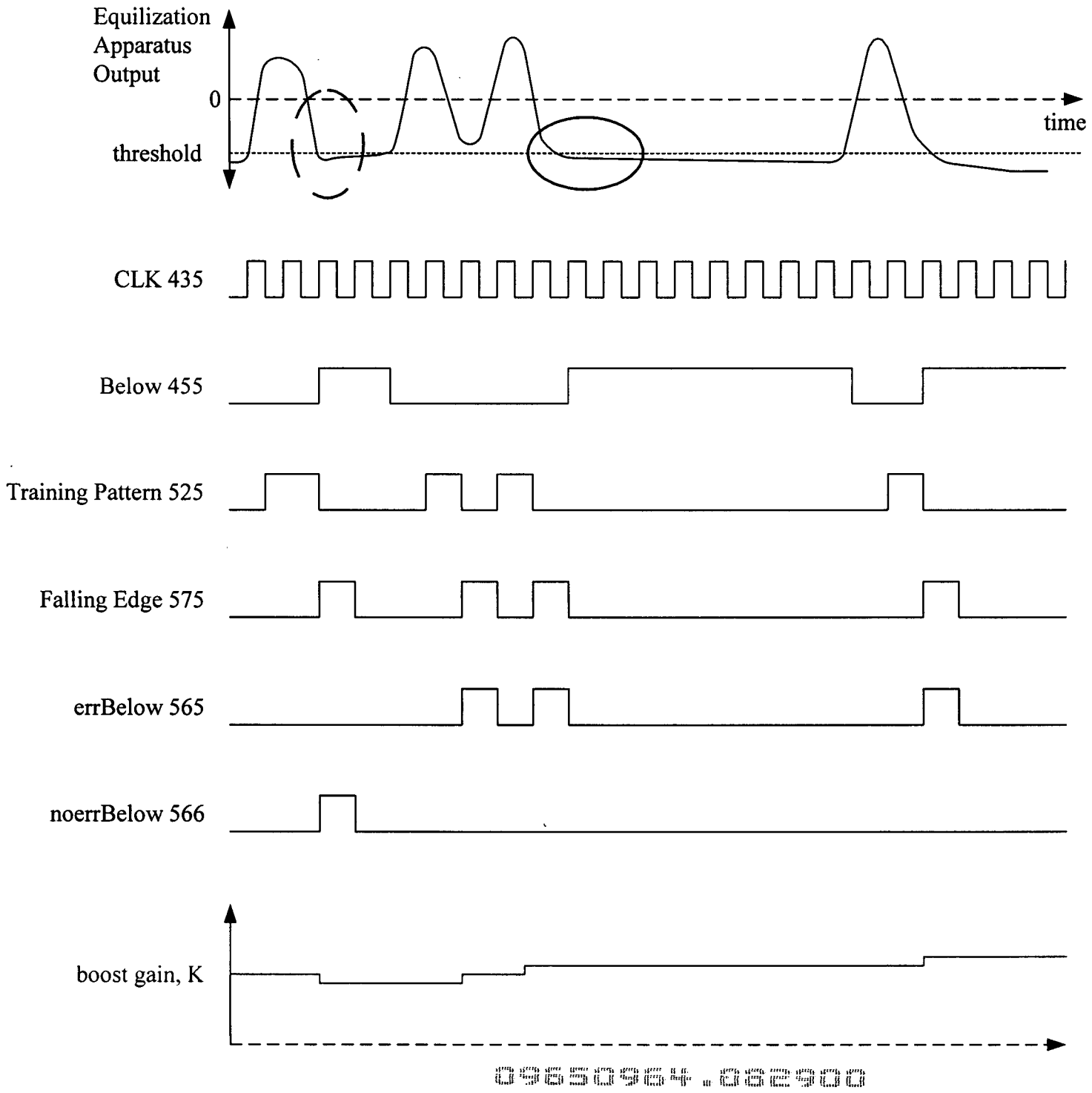

Equilization
Apparatus
Output
0
threshold
time
CLK 435
Below 455
Training Pattern 525
Falling Edge 575
errBelow 565
noerrBelow 566
boost gain, K

FIG. 7

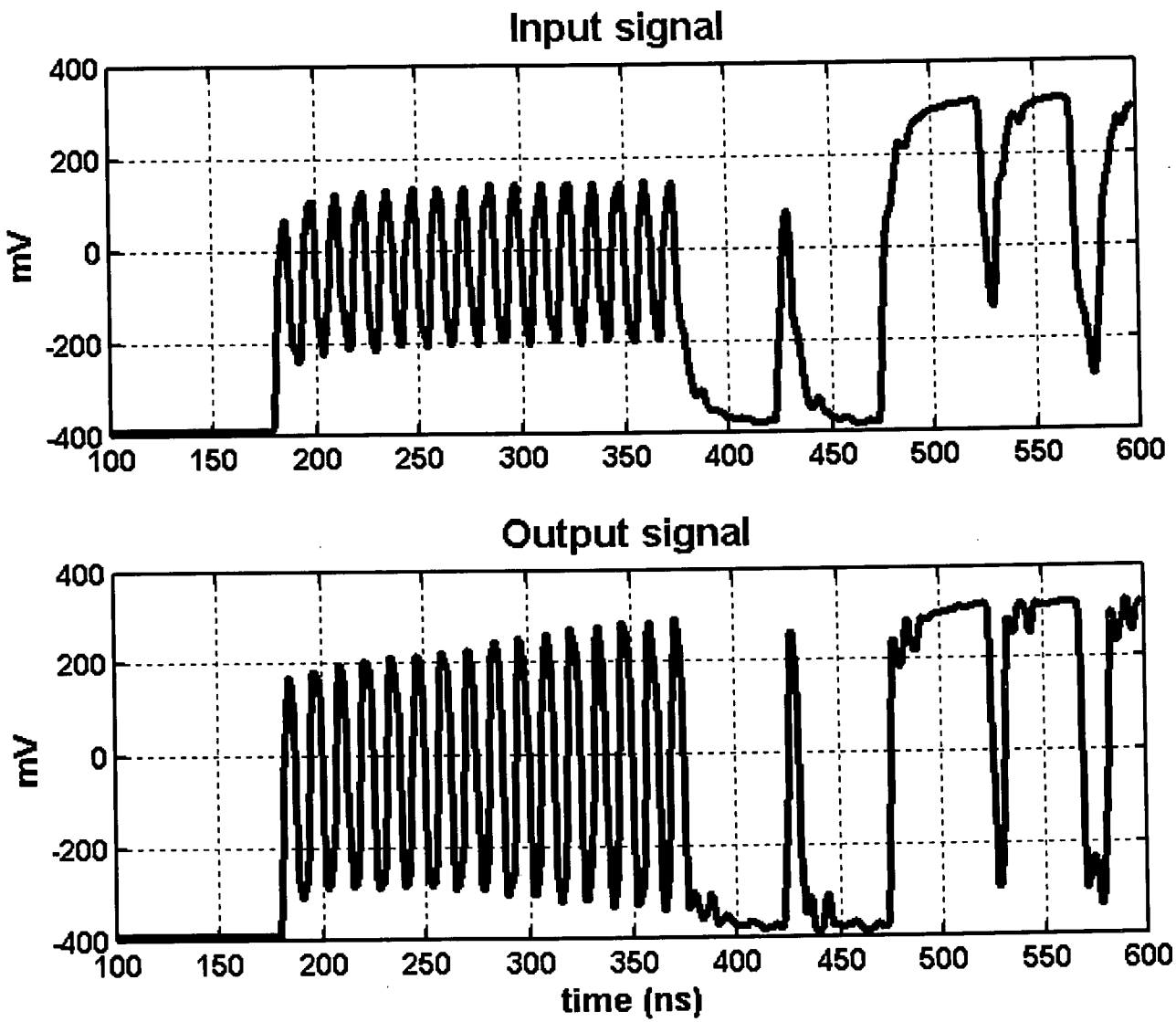

Input signal
400
200
0
-200
-400
mV
100
150
200
250
300
350
400
450
500
550
600
Output signal
400
200
0
-200
-400
mV
100
150
200
250
300
350
400
450
500
550
600
time (ns)

FIG. 8